REMARKS

Restriction Requirement

Applicants hereby affirm the election of Group II, Claims 5-18, for examination in this application without traverse, and cancel Claims 1-4, corresponding to Group I, without prejudice. Such election was earlier provisionally made without traverse by Applicants' attorney, Justin Liu, on April 29, 2005. Applicants reserve the right to resubmit canceled Claims 1-4 in a divisional application.

Summary of Claim Status

Claims 5-18 are pending in the present application after entry of the present amendment. Claims 5-18 are rejected for the reasons discussed below. Applicants respectfully request favorable reconsideration of the claims and withdrawal of the pending rejections in view of the present amendment and in light of the following discussion.

Rejections Under 35 U.S.C. § 112

Claims 5-18 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. With respect to Claims 5 and 18, the Examiner stated:

> First two limitations of the claims 5 and 18 are formulated not clear: if a first signal and a second signal are provided at a data input and at a clock input respectively of the same sequential logic element or different sequential logic elements, since the second limitation of the claim 5 states that the second signal is related to the first signal and according to the Fig. 6A and its description on the Page 14 of the Specification, they are CK1 and CK2 which applied to the different flip-flops 432 and 434.

Office Action at p. 4, ¶ 9.

Applicants respectfully traverse the rejection as to all claims, and submit that the claimed subject matter was described in the specification in accordance with the requirements of 35 U.S.C. § 112. Specifically, Applicants submit that

Claim 5 is clear in reciting that a first and a second signal are provided at a data input and a clock input, respectively, of the same sequential logic element, and Applicants believe Claim 5 is fully supported by the specification.

For example, Applicants refer the Examiner to the example embodiment shown in Figure 4A, where flip-flop 434 of IOB 404 (highlighted with a bold border) may correspond to the sequential logic element. A data input (D) of flip-flop 434 of IOB 404 is coupled to receive a signal P2, and a clock input (>) of the same flip-flop is coupled to receive a signal DP1, which is a delayed version of signal P1. As can be seen in Figure 4A, and as described in the specification, signals P1 and P2 are generated by the same flip-flop (432) in each of IOBs 402 and 404 from a GCK signal and the CK/2 signal. Thus, "the signals P2 and P3 . . . are identical, or nearly so, to the output signal on terminal P1." See Specification at paragraph [0028]. Therefore, since signal P2 is related to P1 (in that they are "identical, or nearly so") and signal P1 is related to DP1 (which is merely a delayed version of P1), signals P2 and DP1, the data and clock inputs, respectively, to flip-flop 434 of IOB 404 are also related, as recited in Claim 5. This relationship between signal P2 and signal DP1 is further shown in the waveform diagram of Figure 4B.

As another example, Applicants refer the Examiner to the example embodiment shown in Fig. 6A, where flip-flop 432 of IOB 404 (highlighted with a bold border) may correspond to the sequential logic element. A data input (D) of flip-flop 432 of IOB 404 is coupled to receive a signal TCK/2, and a clock input (>) of the same flip-flop is coupled to receive a signal CK1. As can be seen in Figure 6A, signal CK1 is merely a delayed version of a test clock signal TCK, and signal TCK/2 is merely the test clock signal TCK divided by two (via clock divider 610). See Specification at paragraph [0045]. Thus, the inputs to flip-flop 432 of IOB 404 are related, since both are derived from the test clock signal TCK. The relationship between the two input signals is also shown in the waveform diagram of Figure 6B.

Therefore, for at least the foregoing reasons, Applicants believe that Claim 5 meets the requirements of 35 U.S.C. § 112 and enables one of skill in the art to

make or use the invention. Applicants respectfully request withdrawal of the rejection and allowance of Claim 5.

With respect to Claim 18, Applicants submit that the language of the claim is clear and meets all statutory requirements. In particular, the first two elements of Claim 18 recite "delivering a first test signal to a data terminal of the logic element" and "delivering a second test signal to a clock terminal of the logic element." As shown in Figure 4A, a first test signal P2 is delivered to a data terminal D of a logic element 434 (of IOB 404), and a second test signal DP1 is delivered to a clock terminal of the same logic element. As another example, Figure 6A shows a first test signal TCK/2 being delivered to a data terminal of a logic element 432 (of IOB 404) and a second test signal CK1 being delivered to a clock terminal of the same logic element. These examples are further explained in the corresponding text of the specification. Therefore, Applicants believe Claim 18 is in compliance with 35 U.S.C. § 112 and enables one skilled in the art to make or use the invention, and Applicants respectfully request withdrawal of the rejection and allowance of Claim 18.

Claims 6-17 are not explicitly addressed in the Office Action, but are assumed to be rejected based on their dependence from Claim 5, and the remainder of this response is based on that assumption. Applicants believe the rejection of Claim 5 has been overcome by the forgoing remarks, and that Claim 5 is allowable. Therefore, Applicants believe Claims 6-17 are also allowable, and allowance of these claims is respectfully requested.

The Examiner further stated that there is insufficient antecedent basis for the limitation "providing a second signal at the clock . . ." in Claim 5, and for the limitation "latching data of the first test signal in the logic . . ." in Claim 18. Applicants thank the Examiner for her close reading of the claims. In response, Applicants have amended Claims 5 and 18 to correct these minor inadvertent clerical errors. Such amendments are not substantive and do not relate to the prior art. Applicants believe the amendments place Claims 5 and 18 in form for allowance, and therefore respectfully request allowance of Claims 5 and 18.

Conclusion

No new matter has been introduced by any of the above amendments. In light of the above amendments and remarks, Applicants believe that Claims 5-18 are in condition for allowance, and allowance of the application is therefore requested. If action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicants' attorney, Justin Liu, at 408-879-4641.

Respectfully submitted,

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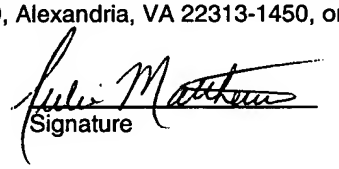
I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450, on August 2, 2005.

Julie Matthews
Name



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